

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS

1. (Currently amended) A method for forming a low resistance MOSFET device comprising the steps of:

forming a gate region atop a surface of a substrate;

forming first spacers having a first spacer width on sidewalls of said gate region;

forming a dopant region comprising source/drain extensions and deep source/drain regions using a single dopant implant step;

forming first silicide regions having a first silicide thickness in said substrate as well as atop a surface of said gate region;

forming second spacers in said substrate and atop a surface of said gate region, wherein said second spacers protect said first silicide region in said substrate; and

forming second silicide regions in said substrate and atop a surface of said gate region, wherein said second silicide regions have a thickness that is greater than said first silicide thickness.

2. (Original) The method of Claim 1 wherein said forming of said gate region further comprises predoping of said gate region.
3. (Original) The method of Claim 2 wherein said predoping is performed by ion implantation of a type III-A element or a type V element into said gate region.
4. (Original) The method of Claim 3 where predoping is achieved via ion implantation of phosphorus into said gate region.
5. (Cancel)
6. (Original) The method of Claim 1 wherein said first spacer width is from about 5 nm to about 20 nm.
7. (Original) The method of Claim 1 wherein said first spacer width is from about 7 nm to about 15 nm.
8. (Original) The method of Claim 1 wherein said second spacers width is from about 20 nm to about 90 nm.
9. (Original) The method of Claim 1 wherein said second spacers width is from about 30 nm to about 70 nm.

10. (Cancel)

11. (Currently amended) The method of Claim [[10]] 1 wherein ~~forming said deep source/drain regions~~ said single dopant implant comprises ion implantation of a type III-A element or a type V element into said substrate.

12. (Original) The method of Claim 1 wherein said forming of said first silicide region comprises depositing a first metal layer upon an exposed surface of said substrate and annealing.

13. (Original) The method of Claim 12 where said first metal layer has a thickness from about 2 nm to about 7 nm.

14. (Original) The method of Claim 13 where said first metal layer comprises Ta, Ti, W, Pt, Co, Ni, or combinations thereof.

15. (Original) The method of Claim 1 wherein said first silicide regions have a thickness of about 1 nm to about 20 nm.

16. (Original) The method of Claim 1 wherein said first silicide regions have a thickness from about 2 nm to about 15 nm.

17. (Original) The method of Claim 1 wherein said first silicide regions have a thickness from about 5 nm to about 12 nm.

18. (Currently amended) The method of Claim 1 wherein said first silicide region is formed in said substrate having a channel region beneath said gate region, where the distance between said first silicide region and said channel region is from about 2 nm to about 15 nm.

19. (Currently amended) The method of Claim 1 wherein said first silicide region is formed in said substrate having a channel region beneath said gate region, where the distance between said first silicide region and said channel region is from about 3 nm to about 10 nm.

Claims 20-33 (Cancelled)

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